What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate;

a resistor element made of silicon and formed over said semiconductor substrate;

a first silicide region and a second silicide region formed over said resistor element; and

first and second contact parts electrically connected to said first and second silicide regions, respectively,

wherein a first length between one end of said resistor element and an end of said first silicide region located on a side facing said second silicide region is longer than a second length between the other end of said resistor element and an end of said second silicide region located on a side facing said first silicide region.

2. The semiconductor device according to claim 1,

wherein a difference between said first length and said second length is set to 5% of or more than the closest length between said first silicide region and said second silicide region.

3. The semiconductor device according to claim 1,

wherein said first silicide region is larger than said second silicide region.

4. The semiconductor device according to claim 1,

wherein a third length between said one end of said resistor element and an end opposite to said end of said first silicide region located on the side facing said

second silicide region is longer than a fourth length between said other end of said resistor element and an end opposite to said end of said second silicide region located on the side facing said first silicide region.

5. The semiconductor device according to claim 4,

wherein a difference between said third length and said fourth length is set to 5% of or more than the closest length between said first silicide region and said second silicide region.

6. The semiconductor device according to claim 4,

wherein a size of said first silicide region is equal to that of said second silicide region.

7. The semiconductor device according to claim 1,

wherein said resistor element is made of a poly-Si layer.

8. The semiconductor device according to claim 7, further comprising:

a bipolar transistor formed over said semiconductor substrate,

wherein said poly-Si layer constituting said resistor element is formed of the same layer as a poly-Si layer constituting a base electrode or an emitter electrode of said bipolar transistor.

9. The semiconductor device according to claim 7, further comprising:

a MISFET formed over said semiconductor substrate,

wherein said poly-Si layer constituting said resistor

element is formed of the same layer as a poly-Si layer constituting a gate electrode of said MISFET.

10. The semiconductor device according to claim 1,

wherein said resistor element is made of a diffusion formed by introducing an impurity into said semiconductor substrate.

11. The semiconductor device according to claim 10, further comprising:

a MISFET formed over said semiconductor substrate,

wherein said diffusion constituting said resistor element is formed of the same layer as diffusions constituting a source region and a drain region of said MISFET.

12. The semiconductor device according to claim 1,

wherein said first silicide region and said second silicide region are made of a cobalt silicide layer, titanium silicide layer, tungsten silicide layer, molybdenum silicide layer, or tantalum silicide layer.

13. The semiconductor device according to claim 1,

wherein said resistor element is a resistor element used in an ECL circuit.

14. The semiconductor device according to claim 1,

wherein said resistor element is a resistor element used in a digital-analog converter.

15. The semiconductor device according to claim 1,

wherein said resistor element is a resistor element used in an RC oscillator circuit.

16. The semiconductor device according to claim 1, wherein said resistor element constitutes a terminal resistor part.

17. A semiconductor device comprising:

a semiconductor substrate;

a first resistor element and a second resistor element made of silicon and formed over said semiconductor substrate;

a first silicide region and a second silicide region formed over said first resistor element, and a third silicide region and a fourth silicide region formed over said second resistor element; and

first, second, third, and fourth contact parts electrically connected to said first, second, third, and fourth silicide regions, respectively,

wherein a difference between a length between one end of said first resistor element and an end of said first silicide region located on a side facing said second silicide region, and a length between the other end of said first resistor element and an end of said second silicide region located on a side facing said first silicide region is larger than a difference between a length between one end of said second resistor element and an end of said third silicide region located on a side facing said fourth silicide region, and a length between the other end of said second resistor element and an end of said fourth silicide region located on a side facing said third silicide region.

18. The semiconductor device according to claim 17, wherein a length of said first resistor element is equal to that of said second resistor element.

19. The semiconductor device according to claim 17, wherein said first and second resistor elements are each formed of a poly-Si layer with the same pattern shape.

20. A manufacturing method of a semiconductor device, comprising the steps of:

preparing a semiconductor substrate;

forming, over said semiconductor substrate, a patterned poly-Si layer for forming a resistor element;

forming an insulator over said poly-Si layer so as to expose a region where a silicide region is to be formed and so as to cover a region where a silicide region is not to be formed;

forming a metal layer over said semiconductor substrate so as to cover said poly-Si layer and said insulator;

performing a thermal treatment to react said metal layer with a part of said poly-Si layer which contacts to said metal layer, thereby forming a first silicide region and a second silicide region over said poly-Si layer; and

forming a first contact part and a second contact part electrically connected to said first silicide region and said second silicide region, respectively,

wherein a length between one end of said poly-Si layer and an end of said first silicide region located on a

side facing said second silicide region is longer than a length between the other end of said poly-Si layer and an end of said second silicide region located on a side facing said first silicide region.